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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Complete if Known

Application Number	10/619,943
Filing Date	July 15, 2003
First Named Inventor	Ingrid Peterson et al.
Art Unit	2624
Examiner Name	Kathleen S. Yuan
Attorney Docket Number	56197200-191/P890

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(Use as many sheets as necessary)***Complete if Known**

Application Number	10/619,943
Filing Date	July 15, 2003
First Named Inventor	Ingrid Peterson et al.
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Sahouria et al., "Full-chip Process Simulation for Silicon DRC," Mentor Graphics, March 2000, 6 pages.	
		Granik et al., "Sub-resolution process windows and yield estimation technique based on detailed full-chip CD simulation," Mentor Graphics, September 2000, 5 pages.	

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